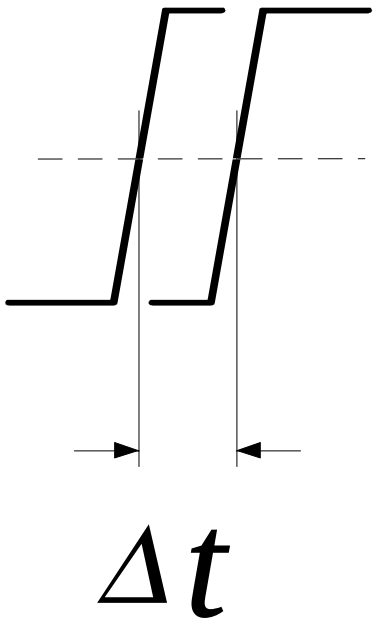
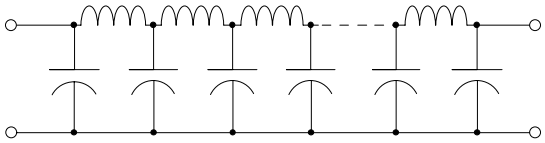
Rhombus Industries Inc.
Transformers & Magnetic Products

1998

Delay Lines



Electromagnetic



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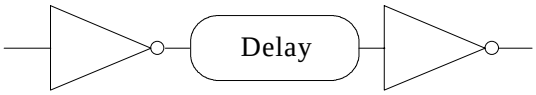

Fast Rise Time
Passives for Impedances from 50 to 200 Ohms

Single / 5 / 10 / 16 / 20 Tap Configurations

Variety of Standard DIP, SIP & SMD Packages

Active Family Logic Types:
FAST / TTL, ACT, LVC & ECL

Special Function:
Programmables, Pulse Width Control Gated Oscillators

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Passive Delay Line Design Considerations

A Passive Delay Line is a special purpose Low Pass Filter designed to delay (phase shift) the input signal by a specified increment of time, and is composed of series inductors and shunt capacitors with values dictated by the line impedance.

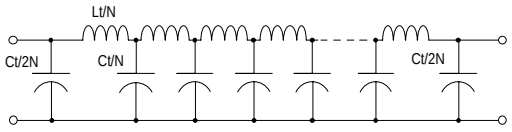

Figure 1A. Passive Delay Line Schematic Diagram.

Design: This LC network may be used to pass either analog or digital signals whose bandwidth is compatible with the intended range of operation for the delay line. A specific delay and impedance, determine the required LC values of the network:

$$Td = \sqrt{(L_t \times C_t)}$$

$$Z_O = \sqrt{(L_t / C_t)}$$

Td = Total Delay (ns)
Z_O = Impedance (Ohms)
L_t = Total Line Inductance (µH)
C_t = Total Line Capacitance (pF)

Rise Time: The rise time of a delay line is typically measured from the 10% to 90% points of the leading edge of the output pulse. The measured output risetime (t_{ro}) is a function of the input rise time (t_{ri}) and the true rise time of the delay line (t_r):

$$t_r = \sqrt{t_{ro}^2 - t_{ri}^2}$$

An analog delay line's bandwidth (-3dB attenuation) is related to the network's rise time which is dependent upon the total number (N) of LC sections. The delay-to-rise time ratio is the figure of merit, or Quality Factor, used to characterize delay lines. Generally, the greater figure of merit implies higher number of sections, and therefore higher cost. The bandwidth for the network, and number of sections follow these approximations:

$$BW \approx .35 / t_r \qquad N \approx (Td / t_r)^{1.36}$$

Attenuation: The output voltage attenuation of a delay line has several contributing factors:

1. Internal D.C. resistance (DCR)
2. Dielectric and ground plane losses
3. Loading effects at taps
4. Impedance mismatches at terminations
5. Frequency limitations (BW) of delay line

When the delay line is minimally loaded, properly terminated and the input pulse widths are significantly greater than the line's rise time, attenuation is given by:

$$\text{Attenuation (\%)} = 1 - (Zo / (Zo + DCR))$$

Series Connection: Passive delay lines of the same impedance can be connected input-to-output (cascaded) to optimize rise time and / or obtain specific delay values. Termination is required only at the output of the final stage. The rise time of the grouped lines is given by

$$t_{ro} = \sqrt{t_{ri}^2 + t_{r1}^2 + t_{r2}^2 + \ldots t_{rN}^2}$$

Operating Specifications - *Passive Delays*	
Pulse Overshoot (Pos)	5% to 10%, typical
Pulse Distortion (S)	3% typical
Working Voltage	25 VDC maximum
Dielectric Strength	100VDC minimum
Insulation Resistance	1,000 MΩ min. @ 100VDC
Temperature Coefficient	70 ppm / °C, typical
Bandwidth (f_C)	$0.35 / t_r$ approx.
Operating Temperature Range	-55° to +125°C
Storage Temperature Range	-65° to +150°C

Reflections: Loading at taps should be at least 10 times the characteristic impedance to minimize reflections due to transmission line effects. The reflected voltage due to a tap loaded by a resistance, R_L, is given by

$$\text{Reflection (\%)} = 1 - (1 / (1 + Zo / 2R_L))$$

In certain applications, mismatches can be used to achieve pulse-shaping requirements. There are three basic rules relating to reflections:

1) No reflections at either terminal of a line which is terminated with its characteristic impedance.

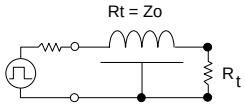

Figure 2A.

2) A reflection, equal in amplitude and of same polarity to the impinging signal, will occur at the input of a line which is open circuited. (R_t = infinite, see figures below.)

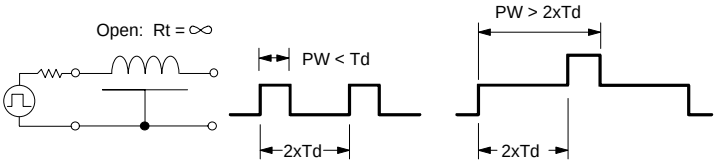

Figure 3A.

3) A reflection, equal in amplitude and of opposite polarity to the impinging signal, will occur at the input of a line which is short circuited. (R_t = 0, see figures below.)

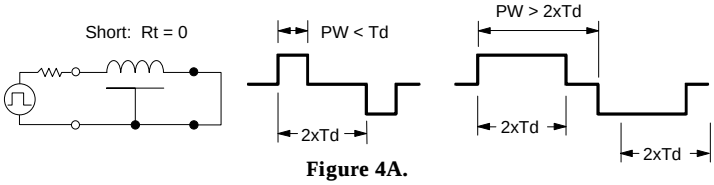

Figure 4A.

Circuit Considerations: To assure delay accuracy and prevent signal distortion, care should be taken to properly integrate the passive delay line into the circuit design. A board trace can load a tap with several picofarads of capacitance which will increase delay, rise time, distortion and attenuation. The designer should calculate inductance and capacitance values of the delay line (L_t , C_t) to determine if anticipated board loading is significant. For typical passive delay line applications, the following design criteria provide optimum performance:

1. The line should be properly terminated.
2. Minimize tap loading. 10 x Z_O min. recommended.
3. Minimize trace lengths to delay line.
4. Circuit should have massive ground plane.
5. All common connections should be used.

We encourage you to call and discuss the details of your design with one of our application engineers. We offer quick turnaround on samples, and custom versions are available, generally at no cost for existing package configurations.

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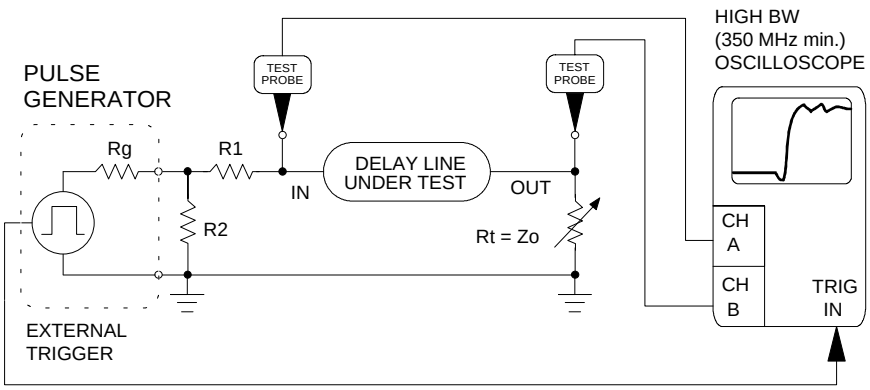


Rg = GENERATOR SOURCE IMPEDANCE = 50 OHMS
R1, R2 = INPUT MATCHING PAD RESISTORS
Rt = TERMINATING RESISTOR
Zo = DELAY LINES CHARACTERISTIC IMPEDANCE

$R1 = \{Rg \times Zo\} / R2$

$R2 = \sqrt{\frac{(Rg^2 \times Zo)}{(Zo - Rg)}}$

Figure 5A. Recommended test circuit for Passive Delay Lines

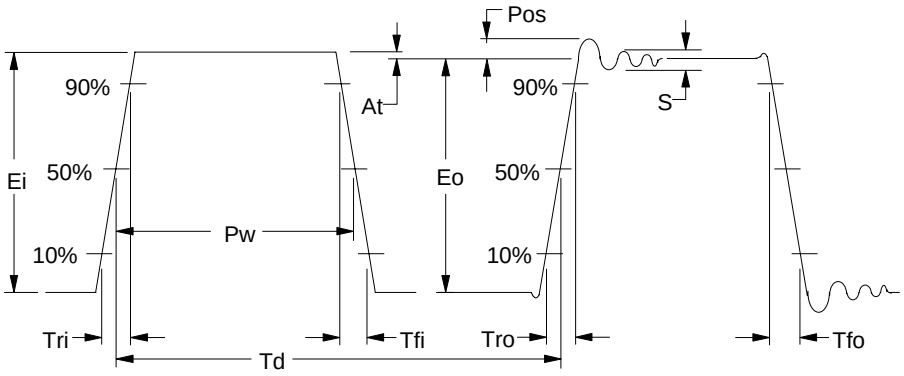


Figure 6A. Passive Delay Line Waveform Parameters

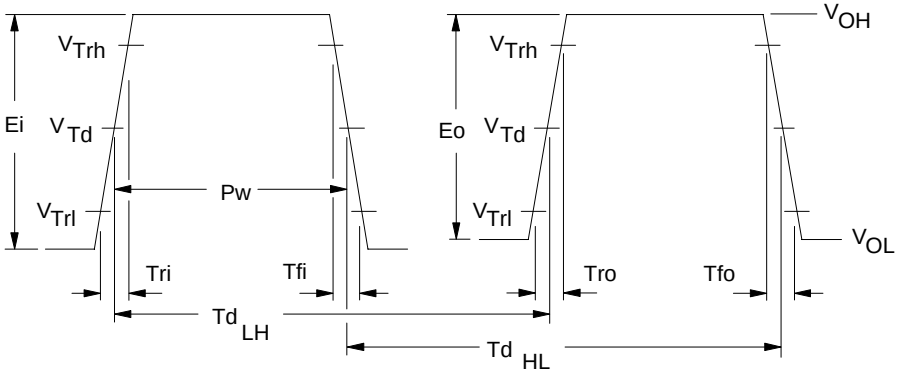


Figure 7A. Active Delay Line Waveform Parameters

GLOSSARY

Attenuation (At): the difference in peak amplitude between input and output pulses.

D.C. RESISTANCE (DCR): The D.C. resistance, in ohms, measured between the input and output of a delay line.

DELAY TIME (Td): the elapsed time between the respective 50% points on the leading edges of the input and output pulses.

IMPEDANCE (Zo): the effective impedance of the delay line which is equal to the value of the terminating impedance which provides a minimum reflection back to the input of the delay line.

INPUT FALL TIME (Tfi): the elapsed time between the 90% and the 10% points on the trailing edge of the input pulse.

INPUT RISE TIME (Tri): the elapsed time between the 10% and the 90% points on the leading edge of the input pulse.

INPUT VOLTAGE (Ei): the amplitude of the input pulse.

LEADING EDGE: that portion of the pulse which rises from zero to peak amplitude.

OUTPUT RISE TIME (Tfo): the elapsed time between the 10% and the 90% points on the leading edge of the output pulse.

OUTPUT FALL TIME (Tfo): the elapsed time between the 90% and the 10% points on the trailing edge of the output pulse.

OUTPUT VOLTAGE (Eo): the amplitude of the output pulse.

PULSE DISTORTION (S): the magnitude of the largest peak amplitude of all spurious responses in either a positive or negative direction occurring in the period after the top of the leading edge of the output pulse and before two time delays (for flat input pulse top).

PULSE OVERSHOOT (Pos): the peak amplitude of overshoot occurring at the top of the leading edge of the output pulse (for flat input pulse top).

PULSE WIDTH (Pw): the elapsed time between the 50% points on the leading and trailing edge of a pulse.

TRAILING EDGE: that portion of the pulse which falls from peak amplitude to zero.

TZB Series High Performance Passive 10-Tap Delay Modules

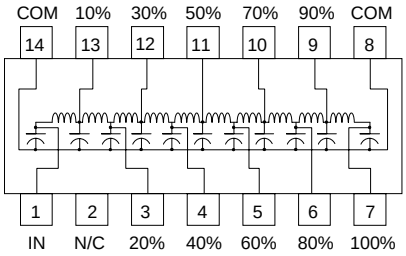
- *Fast Rise Time, Low DCR*
- *High Bandwidth ≈ 0.35 / t_r*
- *Low Distortion LC Network*
- *10 Equal Delay Taps*
- *Standard Impedances: 50 - 75 - 100 - 200 Ω*
- *Stable Delay vs. Temperature: 100 ppm/°C*
- *Operating Temperature Range -55°C to +125°C*

Part Number Description **T *X* B *XX* - *XX***

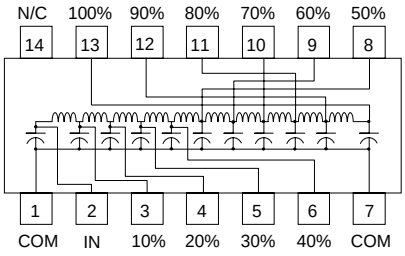
- 14-Pin 10-Tap Delay Line
- Pin Out (Z , Y, U)
- Family Code No. (*See Table for Delay*)
- Line Impedance, Zo (Ohms, ± 5%)
  5 = 50 Ω, 7 = 75 Ω, 10 = 100 Ω, 20 = 200 Ω

Examples: TZB72-5 = Z Style 150ns (15ns per tap) 50 Ω
TUB18-10 = U Style 25ns (2.5ns per tap) 100 Ω

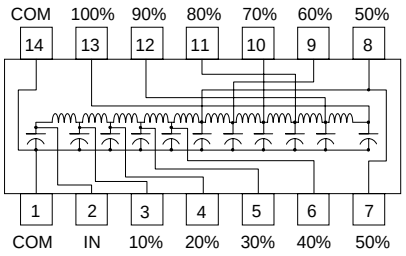
T**Z**B Style Schematic
Most Popular Footprint



T**Y**B Style Schematic
Substitute TYB for TZB in P/N



T**U**B Style Schematic
Substitute TUB for TZB in P/N

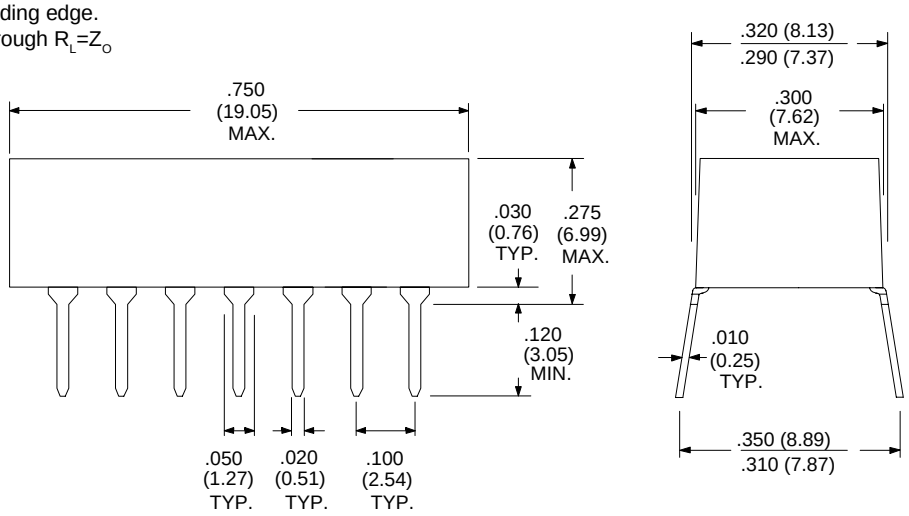


Electrical Specifications at 25°C

Delay Tolerances Total (ns)	Delay Tolerances Tap-to-Tap (ns)	50 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	75 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	100 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)	200 Ohm Part Number	Rise Time (ns)	DCR max. (Ohms)
5 ± 0.5	0.5 ± 0.2	TZB1-5	2.0	0.7	TZB1-7	2.1	0.8	TZB1-10	2.2	0.8	TZB1-20	2.4	0.9
10 ± 0.7	1.0 ± 0.4	TZB6-5	3.2	0.7	TZB6-7	3.6	0.8	TZB6-10	3.8	0.8	TZB6-20	5.5	1.0
20 ± 1.0	2.0 ± 0.5	TZB12-5	4.0	0.7	TZB12-7	4.4	1.3	TZB12-10	4.6	1.5	TZB12-20	8.5	1.5
25 ± 1.25	2.5 ± 0.5	TZB18-5	4.5	0.9	TZB18-7	5.3	1.5	TZB18-10	5.5	1.7	TZB18-20	9.0	1.8
30 ± 1.5	3.0 ± 0.5	TZB24-5	5.5	1.0	TZB24-7	5.8	1.7	TZB24-10	5.8	2.0	TZB24-20	10.0	2.0
40 ± 2.0	4.0 ± 1.0	TZB30-5	7.0	1.2	TZB30-7	7.5	2.0	TZB30-10	7.5	2.2	TZB30-20	13.0	2.2
50 ± 2.5	5.0 ± 1.0	TZB36-5	8.5	1.3	TZB36-7	8.5	2.1	TZB36-10	8.5	2.3	TZB36-20	15.5	2.4
60 ± 3.0	6.0 ± 1.5	TZB42-5	10.5	1.6	TZB42-7	11.4	2.3	TZB42-10	11.5	2.5	TZB42-20	16.0	2.5
70 ± 3.5	7.0 ± 1.5	TZB48-5	11.0	1.7	TZB48-7	13.0	2.5	TZB48-10	13.0	2.8	TZB48-20	17.0	2.5
80 ± 4.0	8.0 ± 1.8	TZB54-5	12.0	1.9	TZB54-7	15.3	3.8	TZB54-10	15.5	3.0	TZB54-20	19.0	2.5
90 ± 4.5	9.0 ± 2.0	TZB60-5	14.0	2.0	TZB60-7	17.3	3.0	TZB60-10	17.5	3.1	TZB60-20	20.0	2.5
100 ± 5.0	10.0 ± 2.0	TZB66-5	18.0	2.1	TZB66-7	19.5	3.1	TZB66-10	20.0	3.2	TZB66-20	24.0	2.5
150 ± 7.50	15.0 ± 3.0	TZB72-5	24.0	2.2	TZB72-7	26.0	3.3	TZB72-10	26.0	3.5	TZB72-20	35.0	3.6
200 ± 10.0	20.0 ± 3.0	TZB78-5	34.0	2.4	TZB78-7	38.0	3.4	TZB78-10	39.0	3.5	TZB78-20	44.0	4.8
250 ± 12.5	25.0 ± 3.0	TZB84-5	41.0	2.4	TZB84-7	45.0	3.5	TZB84-10	46.0	4.0	TZB84-20	56.0	5.2
300 ± 15.0	30.0 ± 3.0	TZB90-5	48.0	2.5	TZB90-7	53.0	3.5	TZB90-10	54.0	4.2	TZB90-20	68.0	5.8
400 ± 20.0	40.0 ± 5.0	TZB94-5	65.0	2.8	TZB94-7	66.0	3.6	TZB94-10	67.0	4.5	———	———	———
500 ± 25.0	50.0 ± 5.0	TZB98-5	75.0	3.3	TZB98-7	84.0	3.7	TZB98-10	86.0	5.0	———	———	———

1. Rise Times are measured from 10% to 90% points.
2. Delay Times measured at 50% points of leading edge.
3. Output (100% Tap) terminated to ground through $R_L=Z_O$

Dimensions in inches (mm)



For other values & Custom Designs, contact factory.

Specifications subject to change without notice.

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